A 16 W PULSED X-BAND SOLID-STATE TRANSMITTER

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ABSTRACT

An X-Band control gain amplifier providing more than 41 dBm CW with 60 dB associated gain and 10 % bandwidth has been developped. The power added efficiency is 15 %. The length of the device is about 100 mm. The transverse dimension is 15 mm, corresponding to a quarter wavelength, compatible with an active X-Band phased array.

At each power level the most appropriate microwave technology has been selected : MMICs, MHMICs (Miniature Hybrid MIcrowave Circuits) or high dielectric constant circuits.

INTRODUCTION

This study which demonstrates the feasability of high power amplifiers is essentially motivated by the needed performances of future one or two axes X-Band phased array antennas designed with solid state T/R modules.

Looking at further applications the device which we developped could be seen as a possible alternative to the first TWT stage of airborne radar transmitters.

These applications make necessary a maximum integration level using FETs with large gate periphery. The design optimizes the efficiency and the thermal resistance of the mounting.

This work has been supported by the French Administration under DRET Contract N° 85/420.

DEVICE DESCRIPTION

The bloc diagramm of the transmitter is given in figure 1. The picture in figure 2 shows the whole ure of the device. Each amplification realized on a carrier to permit the a function or a groupe of functions.

The amplifier design is based on a modular approach. The elementary module is constituted by a 3 W FET chip and two tuning capacitors manufactured on a 100 µm thickness high dielectric constant subtrate (εr = 37).

These components are reported using an eutectic AuSn high temperature solder on a copper heat-sink (3 mm x 3 mm x 3 mm) in order to reduce the thermal resistance. The copper heat-sink is then itself soldered at the bottom of an aluminium package (figure 3).

The 6 W and 12 W amplification stages are realized by combining 2 or 4 elementary hereabove described modules.

LOW POWER AMPLIFIERS

The low power amplifiers are designed using GaAs monolithic technology (1). The first chip, presented in figure 4, is a 15 dB gain amplifier. The second one is a dual-gate FET variable gain amplifier (figure 5). The gain control is over 25 dB with an associated phase variation of 20 degrees. The size of each chip is 2 mm x 1 mm. These MMICs have been manufactured at THOMSON-CSF DAG using 0.5 µm gate length and via-holes technology.

MEDIUM POWER AMPLIFIERS

Up to 1 W output power the MHMICs technology is used (2). The originality of this process consists in prefabricating on an 380 µm thickness alumina substrate and as a continuous sequence of operations a large number of miniature circuits including all the passive elements. Only the active components have to be inserted.

Metallized via holes are available with a diameter of about 300 µm. Ionic etching allows to obtain RLC elements like spiral inductors, interdigital capacitors and resistors. The minimum line and/or gap width we can obtain is 10 µm. MIM capacitors and air-bridges are also available.

The figure 6 shows a picture of a 200 mW amplifier using THOMSON-CSF EC4202 FET. At 1 W power output level we dispose of the THOMSON-CSF V2400 chip (figure 7a). The measured power is shown in figure 7b.

HIGH POWER AMPLIFIERS

The selected power FET used for the realization of the elementary module is FUJITSU FLK502XV. The chip is made of a great number of unit cells (144) with a total gate periphery of 10.8 mm. All these cells are on-chip interconnected using air-bridges. The sources are grounded by via-holes located under connecting pads. Chip area is 2.5 mm x 0.5 mm. The thickness is 60 µm including a 30 µm integrated gold plated heat-sink. All the 3 W, 6 W and 12 W stages have been realized using this high efficiency chip.

The measurements of the 3 W amplifier are given in figure 8. We obtain within a 1 GHz bandwidth 35 dBm output power at 1 dB compression with 7 dB associated gain and about 25 % power added efficiency.

The 6 W and 12 W CW amplifiers were designed using travelling waves dividers and combiners. This type of circuits has been selected according to its major advantage : being of an identical reduced width, whatever the number of FETs to be combined (3). Another advantage compared to in-phase combiners is related to its ability to absorb the reflected waves, due to the phase lags between the different reflected paths, within the surface deposited resistors.

Assuming that they are identical, the individual power stages don't need to be well matched for the overall combined amplifier to have a very low input VSWR. Furthermore, for the first time, this amplifier uses a new design of the TWD concept, particularly suited to high power combining : quarter-wave coupled lines are introduced within the input divider, allowing the insertion of an impedance transformation without any additional length.

Figure 9a shows the circuit description for the 12 W (CW) stage. Figure 9b is a picture of the same circuit. It must be noted that the first run of the modelised design gave the expected result, which confirms an already observed behaviour of the TWD concept, even for such wide bandwidths. The experimental results are given on figure 9c for high level conditions.

PERFORMANCES

The complete transmitter shown in figure 2 has been measured.

The figure 10 presents the 1 dB compression output within the whole frequency range. As can be seen we obtain more than 12 W CW with 60 dB associated gain. The CW power added efficiency is 15 %.

Another fundamental characteristic to be measured is the AM/PM conversion. The figure 11 indicates the phase behaviour for a given compression level for example 25 degrees maximum variation at 1 dB compression point and at 10 GHz.

From CW to extremely fast pulse operations FET power amplifiers provide a host of desirable features. The output power improvements depend on the duty cycle : they are given in figure 12 for various pulse widths from 100 ns to 1 µs.

For instance at 1/20 duty cycle the output power increase of more than 2 dB which leads to peak power levels greater than 16 W.

CONCLUSION

We have demonstrated the feasability of a compact 16 W pulsed, 10 % bandwidth at 10 GHz operating frequency transmitter. The size of the device and the power added efficiency are compatible with airborne phased array antennas constraints.

At each power level we have selected : MMICS for low power stages, MHMICs for medium power stages and high dielectric constant substrate for power amplifiers.

The modular approach associated with the TW combiner design allows, on the near future to replace the 3 W hybrid FET modules by MMICs.

REFERENCES

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1987 International Microwave Symposium Proceeding Brazil.

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TLE Janvier 1987 N° 520.

(3) A. BERT, D. KAMINSKI
"The travelling Wave Divider/Combiner" IEEE Transactions On Microwave Theory and Techniques, MTT, 28 N° 12, December 1980.

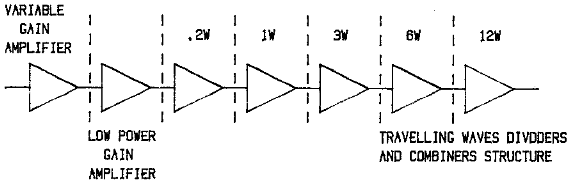

Figure 1 - BLOCK DIAGRAMM OF THE TRANSMITTER

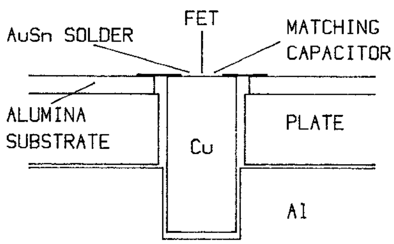

Figure 3 - POWER MOUNTING TECHNOLOGY

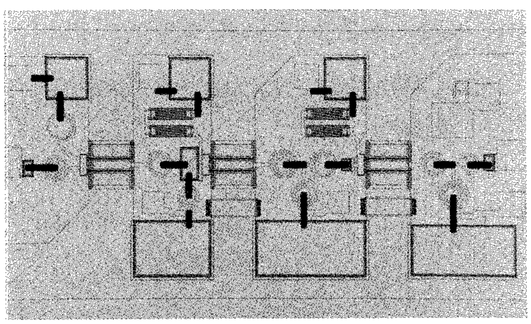

Figure 4 - MONOLITHIC GAIN AMPLIFIER
(2 mm x 1 mm)

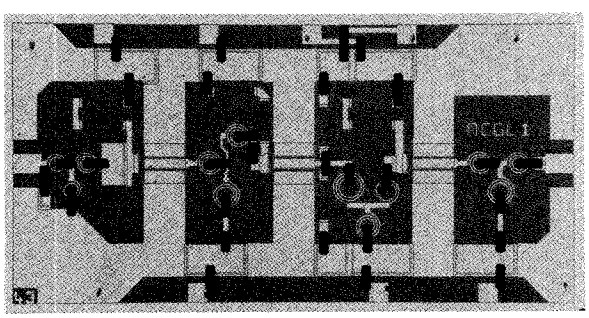

Figure 5 - MONOLITHIC CONTROL GAIN
(2 mm x 1 mm)

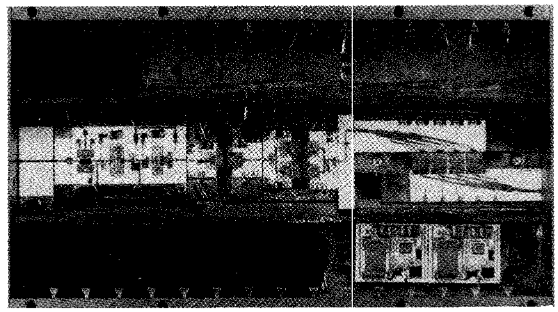

Figure 2 - 16 WATT PULSED X-BAND TRANSMITTER

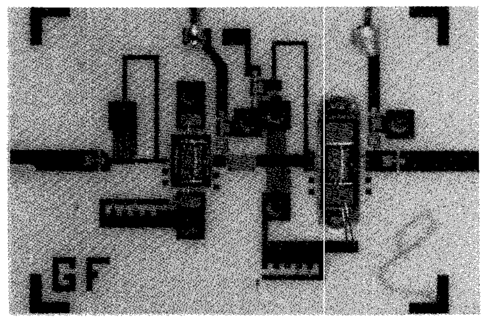

Figure 6 - 200 mW MHMIC AMPLIFIER
(6 mm x 4 mm)

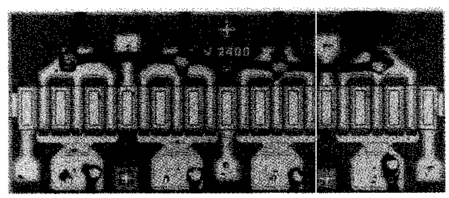

Figure 7a - THOMSON V2400 CHIP

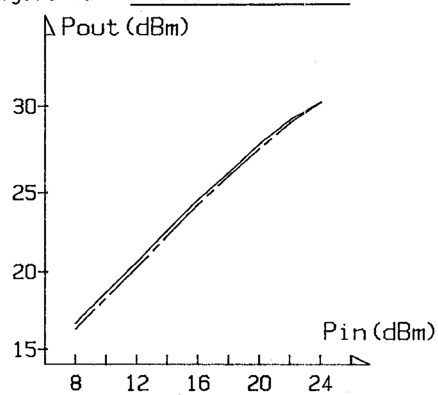

Figure 7b - OUTPUT POWER

Figure 7 - 1 W AMPLIFIER

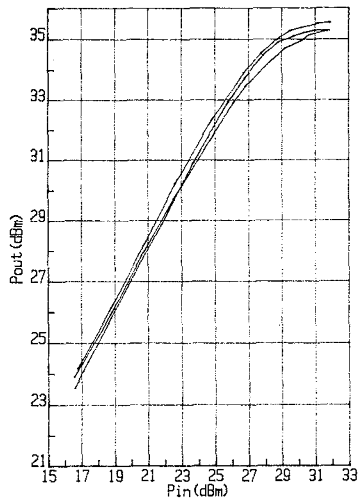

Figure 8 - 3 W AMPLIFIER

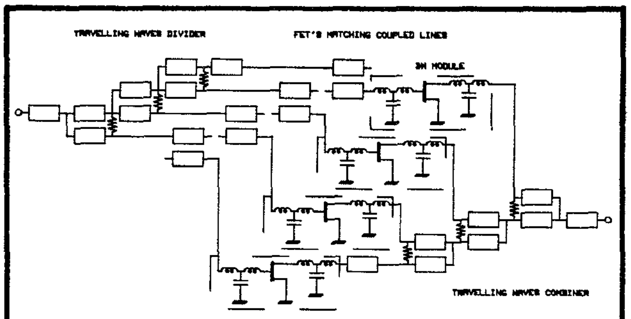

Figure 9a - DESIGN

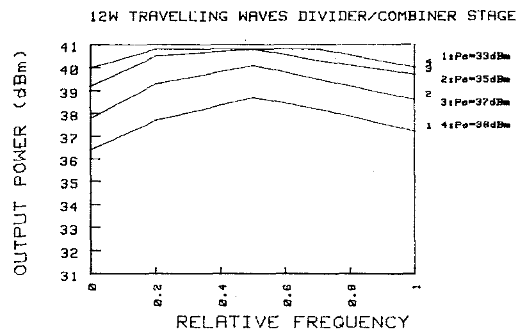

Figure 9c - RESULT

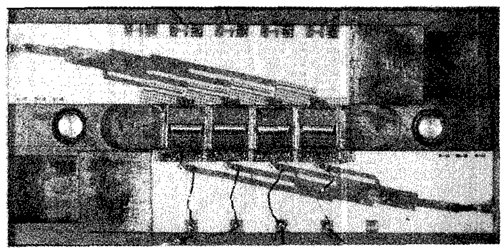

Figure 9b - CIRCUIT

Figure 9 - 12 W CW AMPLIFIER

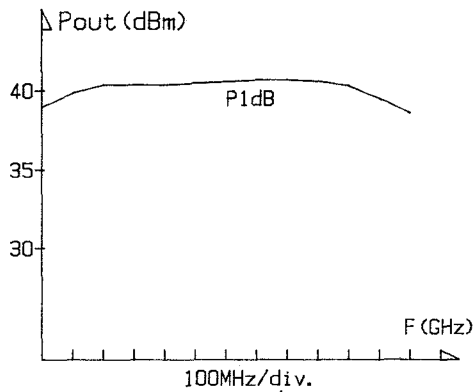

Figure 10 - TRANSMITTER CW OUTPUT POWER

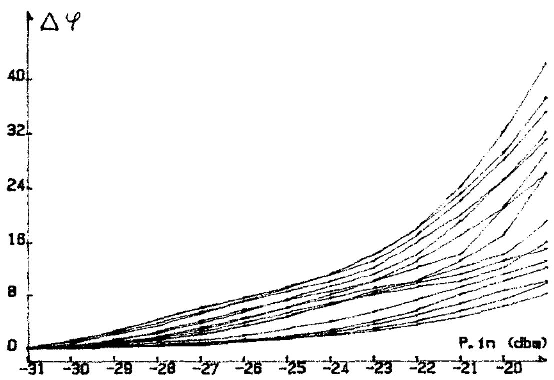

Figure 11 - AM/PM CONVERSION

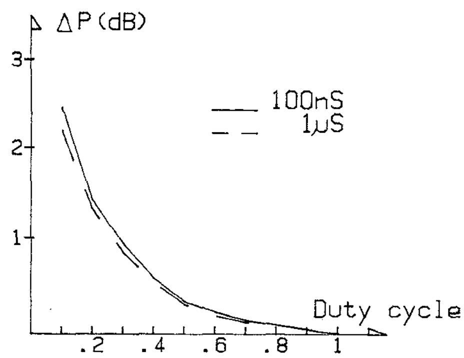

Figure 12 - PULSED TRANSMITTER RESULTS